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Our Docket No.: 98-179/1C - 1496.00065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Jackson L. Ellis et al.		
Application No.:	09/183,694	Examiner:	Park, I.
Filed:	October 30, 1998	Art Group:	2182
For:	COMMAND QUEUEING ENGINE		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 14, 2005.

By: Mary Donna Berkley
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SUPPLEMENTAL REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit the following Supplemental Reply Brief pursuant to 37 C.F.R. §41.41 for consideration by the Board of Patent Appeals and Interferences.

STATUS OF THE APPLICATION

The Board of Patent Appeals and Interferences has designated the application as "special" under MPEP §708.01(D) and thus requires immediate action.[1]

STATUS OF CLAIMS

Claims 3 and 16-26 are pending and remain rejected.

ISSUES

The first issue is whether claims 21, 22 and 26 are patentable under 35 U.S.C. §102(e) over Krakirian, U.S. Patent No. 5,781,803.

The second issue is whether claim 3 is patentable under 35 U.S.C. §103(a) over Krakirian in view of Jones et al., U.S. Patent No. 5,483,641.

The third issue is whether claims 16-20 are patentable under 35 U.S.C. §103(a) over Krakirian in view of Jones et al. and in further view of Bean et al., U.S. Patent No. 4,543,626.

The fourth issue is whether claims 23-25 are patentable under 35 U.S.C. §103(a) over Krakirian in view of Bean et al.

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[1] Remand to the Examiner, Paper No. 34, page 2.

ARGUMENTS IN RESPONSE TO SUPPLEMENTAL EXAMINER'S ANSWER

Regarding claim 21, the Examiner notes that elements of the application, such as a microprocessor and firmware (part of a data controller), may perform some command reordering.[2] However, the Examiner does not provide any evidence that a data controller disclosed in the application cannot perform reordering. In contrast, the application states, "For example, the TE entry can contain all the information in the received command. In that case, CQE 215 can directly set up the necessary context for data transfer **without firmware intervention.**"[3] (Emphasis added.) Furthermore, FIG. 2 of the application shows that the command queue engine (CQE) 215 is part of a data controller. Therefore, the Examiner's assertion that the claimed "data controller" does not actually mean a disclosed data controller appears to be incorrect.

The Examiner further argues that command reordering is performed by a CFIFO 217 in Krakirian.[4] In contrast, Krakirian describes the CFIFO 217 as "a 16×8 array of registers."[5] One of ordinary skill in the art would not appear to understand that an array of registers could minimize interrupts to a processor by re-ordering a plurality of commands received from a host computer from an order of arrival to an order of sequence in a storage medium as presently claimed. Register arrays commonly store data when written to and present data when read from. Therefore, Krakirian does not appear to expressly or inherently discloses all of the claimed elements as arranged in the claim.

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[2] Examiner's Supplemental Answer, 20 May 2005, page 9, point a).

[3] Application, page 47, lines 4-7.

[4] Examiner's Supplemental Answer, 20 May 2005, page 9, point a).

[5] Krakirian, column 7, line 58.

The Examiner further argues that Krakirian discusses eliminating at least one interrupt to a microprocessor 206.[6] In contrast, no evidence is provided that (i) the eliminated at least one interrupt is due to operations of a data controller as presently claimed, (ii) the eliminated at least one interrupt is achieved by reordering a plurality of commands as presently claimed or (iii) eliminating the at least one interrupt minimizes interrupts to a processor as presently claimed. Therefore, Krakirian does not appear to expressly or inherently discloses all of the claimed elements as arranged in the claims. As such, the rejection of claim 21 should be reversed.

Regarding claim 26, the Examiner alleges that Krakirian discusses creating two threads of a plurality of commands, one thread in column 12, lines 58-67 and another thread in column 4, lines 19-23.[7] However, the cited text of Krakirian only appears to discuss **a single command**:

> At location 13h, execution of the NOP with the B_AUTO branch condition results in the sequencer determining whether **the command** in the CFIFO requires microprocessor intervention or whether **the command** in the CFIFO should be executed without microprocessor intervention. In order for the SCSI interface portion 211 to determine that it should carry out **the command** without microprocessor intervention, **the command** must be either an autowrite command as indicated by an autowrite bit AWR in register HSTATO being set or an ESP command as indicated by an ESP bit in register HSTATO being set. In the presently described scenario, **the command** is an autowrite command. Three conditions must be met in order for the sequencer to automatically branch to the data transfer phase in the presently described scenario.[8] (Emphasis added)

Nowhere in the above text does Krakirian appear to mention creating one of multiple threads **of a plurality of commands** and generating interrupts at the beginning and end of the plurality of

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[6] Examiner's Supplemental Answer, 20 May 2005, page 10, point b).

[7] Examiner's Supplemental Answer, 20 May 2005, page 10, point c).

[8] Krakirian, column 12, line 58-column 13, line 5.

commands relative to a data transfer as presently claimed. Therefore, Krakirian does not appear to expressly or inherently disclose all of the claimed elements as arranged in the claims. As such, the rejection of claim 26 should be reversed.

Regarding claim 3, the Examiner argues that one of ordinary skill in the art would be "easily motivated" to modify the queue of Krakirian.[9] However, no clear and particular evidence of motivation is provided from (i) any of the references, (ii) knowledge generally available to one of ordinary skill in the art or (iii) the nature of a problem to be solved. The alleged motivation appears to be merely a conclusory statement. Therefore, *prima facie* obviousness has not been established for lack of clear and particular evidence of motivation to combine and/or modify the references. As such, the rejection of claim 3 should be reversed.

CONCLUSION

The Examiner fails to shown that Krakirian expressly or inherently discloses all of the claim elements as arranged in claims 21 and 26. The Examiner fails to provided clear and particular evidence of motivation to combine Krakirian and Jones et al. in the rejection of claim 3. Therefore, the Examiner has not established a *prima facie* cases in rejecting each of the independent claims. It is respectfully requested that the Board overturn the Examiner's rejections for all of pending claims 3 and 16-26 and hold that the claims are not rendered anticipated or obvious by the cited references. However, should the Board find the arguments herein in support of independent

[9] Examiner's Supplemental Answer, 20 May 2005, page 11, last sentence.

claims 3, 21 and/or 26 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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Dated: July 14, 2005

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